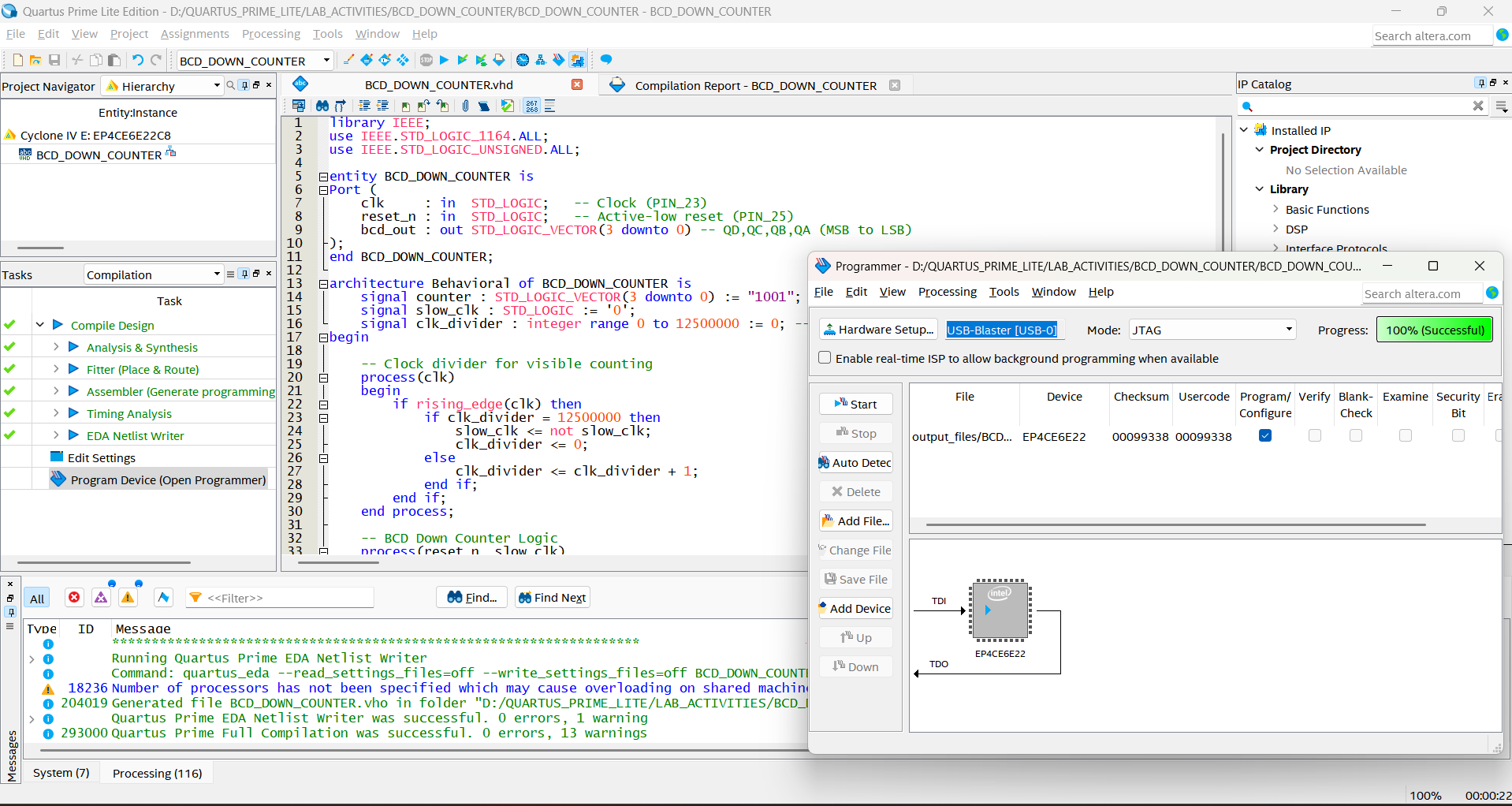
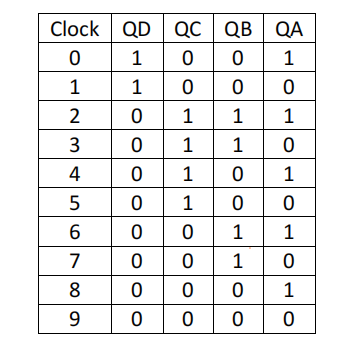
Name: Richard Raymond J. Canda

C.Y.S.: BSCpE - 3A





**BCD DOWN COUNTER:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity BCD\_DOWN\_COUNTER is

Port (

clk : in STD\_LOGIC; -- Clock (PIN\_23)

reset\_n : in STD\_LOGIC; -- Active-low reset (PIN\_25)

bcd\_out : out STD\_LOGIC\_VECTOR(3 downto 0) -- QD,QC,QB,QA (MSB to LSB)

);

end BCD\_DOWN\_COUNTER;

architecture Behavioral of BCD\_DOWN\_COUNTER is

signal counter : STD\_LOGIC\_VECTOR(3 downto 0) := "1001"; -- Start at 9

signal slow\_clk : STD\_LOGIC := '0';

signal clk\_divider : integer range 0 to 12500000 := 0; -- 2Hz @ 50MHz

begin

-- Clock divider for visible counting

process(clk)

begin

if rising\_edge(clk) then

if clk\_divider = 12500000 then

slow\_clk <= not slow\_clk;

clk\_divider <= 0;

else

clk\_divider <= clk\_divider + 1;

end if;

end if;

end process;

-- BCD Down Counter Logic

process(reset\_n, slow\_clk)

begin

if reset\_n = '0' then

counter <= "1001"; -- Reset to 9

elsif rising\_edge(slow\_clk) then

if counter = "0000" then -- 0 in decimal

counter <= "1001"; -- Reset to 9

else

counter <= counter - 1; -- Decrement

end if;

end if;

end process;

-- Active-low LED output (0=LED ON, 1=LED OFF)

bcd\_out <= not counter;

end Behavioral;